WHAT IS CLAIMED IS:

1. A bus control method for a bus, which is provided with a switch having a plurality of master ports and a plurality of slave ports and can connect each of the plurality of master ports to an arbitrary port of the plurality of slave ports, comprising:

an address phase which issues an address and a command; and

a data phase which is separated from the address phase and issues write data,

wherein an address phase of next transaction can be issued before the data phase is completed.

2. The bus control method according to claim 1, wherein

a read return signal is prepared besides the address and the command, and read return data is separated from an address and a command transmitted from a master and switched.

3. The bus control method according to claim 2, wherein

a transaction is issued in the same sequence in single and burst transactions or read and write transactions.

4. The bus control method according to claim 2,

wherein

a start signal of a transaction is used also as a request signal for the switch.

5. A bus comprising:

a switch, which can connect each of a plurality of master ports and an arbitrary port of a plurality of slave ports, wherein

an address phase that issues an address and a command, and a data phase that issues write data are separated, and an address phase of next transaction can be issued before the data phase is completed.